"Smart" source, mask, and target co-optimization to improve design related lithographically weak spots

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ABSTRACT

As patterns shrink to physical limits, advanced Resolution Enhancement Technologies (RET) encounter increasing challenges to ensure a manufacturable Process Window (PW). Moreover, due to the wide variety of pattern constructs for logic device layers, lithographically weak patterns (spots) become a difficult obstacle despite Source and Mask co-Optimization (SMO) and advanced OPC being applied. In order to overcome these design related lithographically weak spots, designers need lithography based simulator feedback to develop robust design rules and RET/OPC engineers must co-optimize the overall imaging capability and corresponding design lithography target. To meet these needs, a new optimization method called SmartDRO (Design Rule Optimization) has been developed. SmartDRO utilizes SMO's Continuous Transmission Mask (CTM) methodology and optimization algorithm including design target variables in the cost function. This optimizer finds the recommended lithography based target using the SMO engine. In this paper, we introduce a new optimization flow incorporating this SmartDRO capability to optimize the target layout within the cell to improve the manufacturable process window. With this new methodology, the most advanced L/S patterns such as metal (k1 = 0.28) and the most challenging contact patterns such as via (k1 = 0.33) are enabled and meet process window requirements.

Keywords: RET, manufacturable PW, SMO, SmartDRO, CTM, Design (Layout) Optimization

1. INTRODUCTION

For sub-20nm technology nodes, the patterning capability of hyper-NA ArF immersion scanners is very close to the physical resolution limit for manufacturability. To help address this challenge, the most advanced RETs have been adopted including SMO [1,2,3,4] and MBSRAF (Model-Based Sub-Resolution Assist Features) [5]. However, despite using these advanced RETs, there are still unresolved lithographically weak patterns. These patterns are categorized as 'design related' hot spot patterns because SMO and MBSRAF have already been used as litho-process optimization solutions, including the use of the advanced continuous transmission mask (CTM) algorithm in SMO. Consequently, target design optimization is required during the OPC step [4,6,7], however current DFM solutions for patterning are not well optimized within the current limited capabilities of the design modification environment. This is due to the fact that sub-20nm device products are very sensitive to chip size to ensure cost-effective chip design. This means the design/target modification to improve the patterning margin is constrained from a chip area point of view.

Therefore, these design related hot spot patterns should be resolved using a new methodology of co-optimizing the design layout and mask (OPC), including minimizing the chip area increase as well. This new methodology adopts SmartDRO for lithography performance-based design rule exploration, optimization and analysis. It utilizes SMO's CTM methodology as the foundation of the design target and advanced RET co-optimization. Most importantly, as we pointed out for the cost-effective chip design, SmartDRO has an unique advantage for the cell design optimization that it does not require cell size increase because it optimizes the design target within the cell area. In this paper, the aforementioned

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new methodology of design layout optimization is studied to find the optimum design layout target with the best manufacturable process window. The design layout target optimization flow is composed of the following steps:

1) We verify the original design layout utilizing an OPC verification tool (Lithography Manufacturability Check - LMC) or from wafer exposure data.
2) Lithographically weak patterns (hotspots) are identified during the first step.
3) A design rule target optimization (SmartDRO) job is setup including these lithographically weakspots clips.
4) During the design rule optimization step, the weak patterns' target layer is optimized resulting in a new target layout.
5) There are two possible approaches depending on the pattern type. For standard cell layouts used for front end of line (FEOL), designers will use this lithography based simulation feedback to re-draw the cell design accordingly and replace the original cells. The optimization results can also be analyzed and applied to the OPC recipe instead of the standard cell modification.
6) For back end of line (BEOL) metal routing layers, on the other hand, because the original design has been generated by an automatic routing tool, rules from the optimized layout are extracted. A pattern search and match tool is used to find all the similar patterns in the layout and the targets are modified using the newly generated rules based on the DRO generated recommendations.
7) Next is to setup the re-OPC using the newly optimized target layout and tuned OPC recipe in either case.
8) After the re-OPC is done, the results are analyzed and compared with the original pre-DRO results to decide if the changes are acceptable as improvements or not.
9) In case there are new hotspots found or certain patterns printability does not improved, the flow will be repeated.

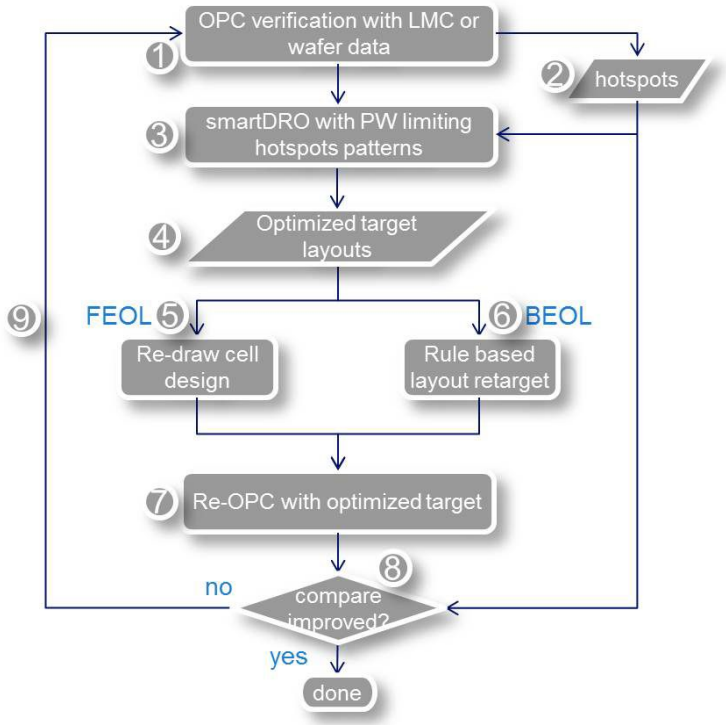

Figure 1. Flow chart for describing the design layout optimization flow. Lithographically weak spots such as PW limiting patterns are used to setup the SmartDRO job. After the job is done, DRO will output optimized new target layouts for re-OPC and results analysis.

Figure 1 illustrates this design layout optimization flow. Using this flow, we demonstrate low k1 imaging improvements to gain manufacturable process windows for both standard (STD) cell and random patterning for sub-20nm logic metal routing layers. In following section, we briefly introduce the mathematical background of SMO and DRO algorithm and description on how to setup the design dimension for the design optimization in DRO. Section Three of this paper presents the main results on sub-20nm metal routing patterns and STD cell case followed by conclusion in section Four.

2. DESIGN RULE OPTIMIZATION ALGORITHM

SmartDRO shares the same basic optimization algorithm with the standard SMO but now includes the addition of the design/target variables in the optimization cost function and constraints. We start with the description of the cost function and algorithm in a standard SMO application first. In SMO, the source and mask co-optimization is derived from an intuitive cost function based on edge placement error (EPE) through all evaluation points and all process window conditions [3] by:

$$s(v_{src}, v_{mask}) = \sum_{pw,eval} \left(w_{pw} w_{eval} \mid EPE_{pw,eval} \mid^2 \right)^{p/2} \qquad \text{Equation 1}$$

Where, S represents the cost function of variables for the source and the mask, pw is the user defined process window conditions for evaluating the cost function during the optimization. Another variable $eval$ represents a set of evaluation points on the design target and the value p is the power. The weighting factor, w_{pw},w_{eval} indicates the weight distribution of each evaluation point within the process windows. This cost function is EPE-based and it calculates the sum of $|\text{EPE}|^p$ for all evaluation points ($eval$) and all process window (pw) conditions with user specified weighting factors, w.

The objective of the optimization is essentially to minimize the EPE across all evaluation points and all process window conditions (see Figure 2). Process window conditions considered in the optimization include delta dose, defocus and mask error which optimize exposure latitude (EL) or normalized image log slope (NILS), depth of focus (DOF) and mask error enhancement factor (MEEF) respectively. A multi-dimensional process condition matrix is achieved by introducing two dose, defocus and mask error settings in each direction of the process window conditions. The advantage of co-optimization over an iterative method is that it is less probable to end up in a local minimum, especially for the case with multiple degrees of freedom for source and mask optimization. It is already known that the co-optimization method provides significant process window improvement over iterative approach [3].

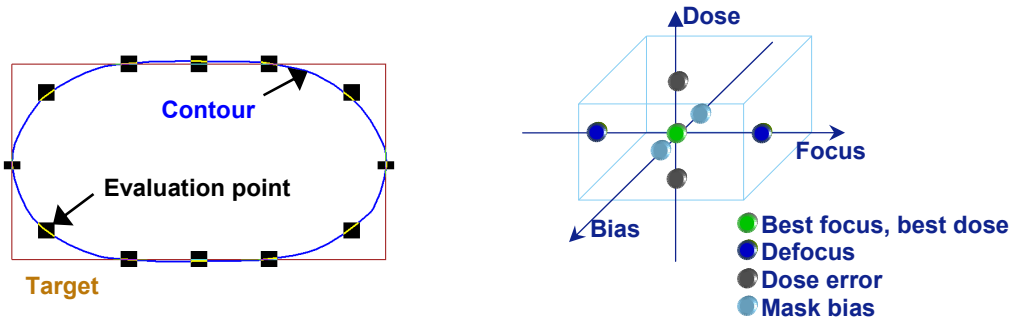

Figure 2: EPE is minimized at each evaluation points through process window conditions. Process window condition is determined by a three dimensional matrix of dose, defocus and mask bias conditions.

For DRO application, we define the cost function by adding the design related variable into the SMO cost function as:

$$s(v_{src}, v_{mask}, v_{design}) = \sum_{pw,eval} \left(w_{pw} w_{eval} \mid EPE_{pw,eval} \mid^2 \right)^{p/2} \qquad \text{Equation 2}$$

Therefore, as shown in Equation 2, the optimization algorithm is very similar to SMO with an additional variable in the cost function "design". In practice, we can define a set of design rule parameters and optimization constraints and relate

them to the target design to co-optimize the source, mask and design/target during SMO. This means that, design rule parameters and related target design edges are treated as optimization variables and are co-optimized with the source and mask variables. As with standard SMO, the EPE-based cost function is evaluated through all process conditions and minimized during the optimization. The final output includes the optimized design rule parameters, target designs and updated metrology in addition to the optimized source and mask. In DRO, by default, unless it is disabled explicitly in the flow, the design/target optimization is turned on when the design rule parameters and related dimensions for the target designs are defined. This behavior is consistent with the default behavior for source and mask variables. To achieve best results for this integrated DRO with SMO algorithm, we use customized DRO flow to co-optimize design/target, source and mask simultaneously for the DRO purpose.

3. RESULTS ANAYSIS

3.1 Metal routing patterns

We first demonstrate the optimization flow and results for 20nm metal routing patterns. We collected lithographically weak spots from either wafer data or simulation results for the POR (process of record). Then, as described in the previous section, a DRO job is performed using these weak pattern clips and with three dimensional process conditions in this case: +/-30nm delta focus, +/-4% delta dose and +/- 0.5nm mask errors. The optimal ranges of these process window conditions are defined during the optimization by iterating the DRO jobs after the first job is done with the default settings. Another important point during the DRO job setup is that the weak points to be re-targeted should be identified by drawing cut-lines on the original target edges of the weak patterns. Therefore, we identified the lithographically weak points and the target layout is optimized to improve the overall litho-performance. For measuring the litho-performance improvements, we compare the original defects (bridging or necking) captured in the original OPC verification job (baseline LMC) or compare PV (process variation) band before and after the target optimization. Even though the mask layers are also optimized during the DRO stage, there are only a limited number of clips. In order to ensure full-chip coverage, we perform a rule based layer retargeting using the newly generated rules based on the DRO recommendation. In sequence, a pattern search and match tool for full chip level will find all locations which fall into the same category as we find in the DRO job and match the rules accordingly. Then, we are ready to do full chip OPC with the new target layout.

We found consistent litho-performance improvement results using the new OPC with newly generated rules based on the DRO recommendations. One example of lithographically weak spots from a typical metal routing layer is shown in Figure 3. We have seen that the PV bands after DRO are substantially improved from the original POR case.

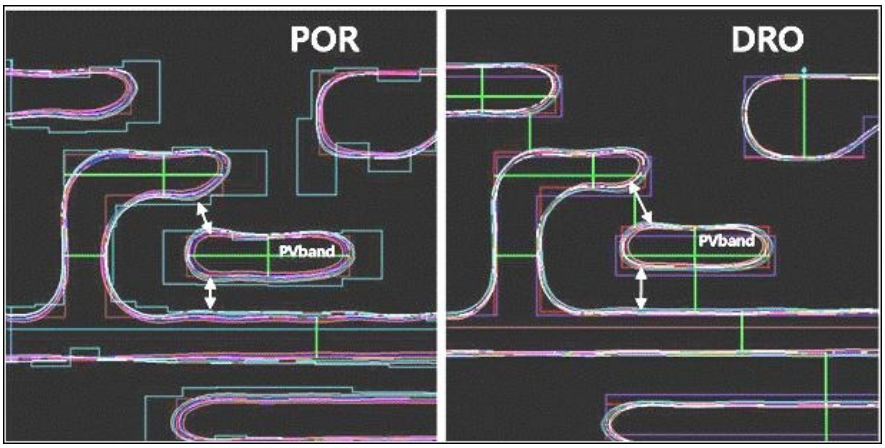

Figure 3. Typical weak spots in the metal routing patterns used to check the litho-performance improvements. We compare the PV bands for the POR and DRO results. All of the weak spots are improved after re-OPC using the 'optimized' target from DRO output.

We further studied the input design dependency on DRO performance by comparing results from two different cases: We pre-treated the input target design using 'rule based retargeting' process for the DRO run (before step 3 in Figure 1) and continue the design layout optimization until step 7 in Figure 1. We then compare this result with the previous case where there is no modification of the input design before DRO. We found that the no modification on the input design case yields better litho-performance in most cases i.e. smaller PV bands and original defects (bridging or necking) were fixed or improved. This is due to the fact that when there is more freedom for the optimizer to optimize the cost variables, it takes full advantage of the DRO capabilities resulting in lithographically more robust solutions. Table 1. summarizes the improvements for the selected cases and compares DRO using the modified target input (DRO^1) and DRO using the original target input (DRO^2).

Table 1. PV band comparison for selected cases. DRO^1 is the flow using the target after rule based retargeting process as DRO input. DRO^2 is the flow using the original target as DRO input. We see a reduction of PV band for all weak spots, many of which are substantially improved compared to POR PV band.

weak spots	*POR*	*DRO^1*	*DRO^2*	*improvements*
1	25.43nm		14.29nm	44%
2	13.80nm		12.69nm	8%
3	12.92nm		7.41nm	43%
4	12.69nm		9.05nm	29%
5	20.82nm		10.72nm	49%
6	16.03nm		9.86nm	38%
7	15.09nm	14.23nm	9.97nm	7%[1] / 34%[2]
8	16.09nm	13.38nm	7.90nm	17%[1] / 51%[2]

3.2 Standard cell

Typical standard cell design optimization in DFM point of view is to prevent the lithographically weak spots using litho-patterning simulation feedback. However, sub-20nm technology nodes require more advanced optimization flows to maximize the lithography patterning process window especially for standard (STD) cell area. The STD cell is one of the key limiters for litho-patterning margin in these technology nodes. Moreover, the chip size is a very important factor for price competitiveness. Therefore, a new method to optimize the patterning process window without growing the cell size is highly desired. In order to achieve this, we adopt SmartDRO in the standard cell design stage to maximize the patterning process window without increasing the cell size.

For this STD cell case, we had multiple lithographically weak patterns in the original cell design, in particular, hook patterns that face each other have small litho-patterning margin due to the strong MRC limitation after OPC. In order to overcome this, we decide to optimize the cell design. We verified multiple STD cell's weak points with the OPC verification tool and run the design optimization flow. Practically, DRO job setup and tuning during the design optimization flow is the same as the metal routing layer case. After the optimization is done, we compared PV band and original defects as done with the previous case. This work is done with simulation results only; we first checked the optimized design layout and observed all the limiting design patterns became more relaxed widths and spaces. As a result, we found moderate but consistent PV band improvements from DRO versus POR for all weak points. Figure 4 compares PV band and design width (CD) for original target (POR) and retarget after the DRO and shows the improvements from DRO. It is also clearly shown that DRO suggests the largest possible target design rule for the design width (CD) allowed by DRC limit in order to maximize the litho-performance improvements.

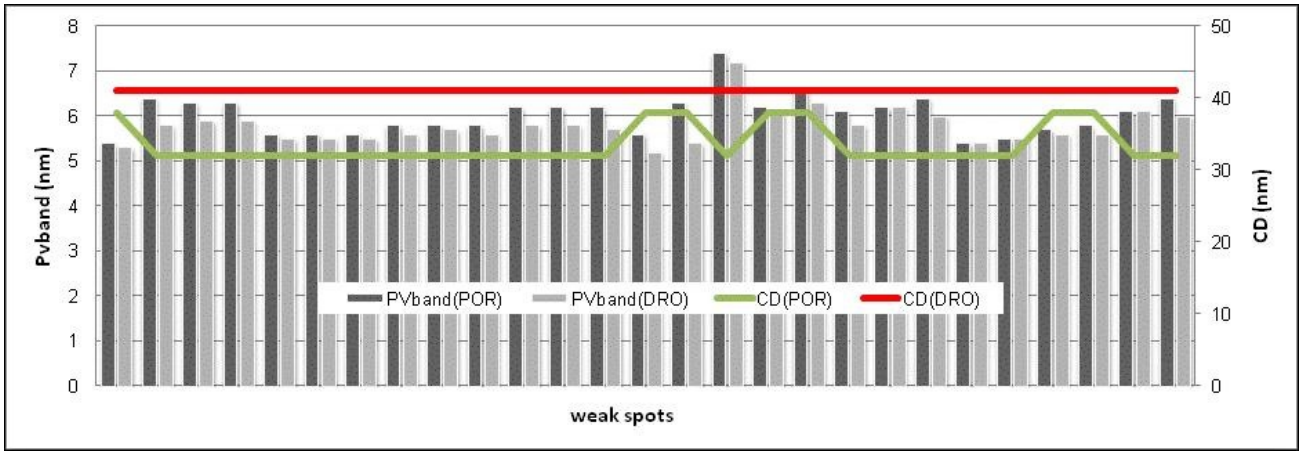

Figure 4. Comparison of PV band and design width (CD) before and after DRO for all weak spots in the STD cell. Lithographically weak spots are improved moderately but consistently after OPC using newly 'optimized' cell design from DRO output. DRO suggest the largest possible target design rule (red line) to maximize the improvements.

4. CONCLUSION

We demonstrate several advantages to using an optimized target based on DRO generated recommendations from our design layout optimization flow. For this sub-20nm tech-node, we show the lithographically weak spots from both the metal routing layer and STD cell design have been successfully improved by this design layout optimization flow incorporating SmartDRO capability. In case of metal routing layer, we find substantial improvements in litho-performance by comparing the PV band value and original defects (bridging and necking from the weak spots) have been fixed or improved. We also find that when there is more freedom for the optimizer to optimize the cost variables, it takes full advantage of the DRO capabilities resulting in lithographically more robust solutions. From the STD cell case, we observe moderate but consistent improvements in PV band and DRO suggests the largest possible design rule to maximize the litho-performance improvements in this leading edge technology device. In addition to this, the new optimization flow ensures the optimal sizes for critical features and increases manufacturable process window without increasing the cell or chip area.

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